CLAIMS

1. (Original) A communications channel system for using fibre-channel cyclic-redundancy code (CRC) for data integrity in an on-chip memory comprising:

   a first channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

   an on-chip frame memory located on-chip in the first channel node that receives a frame and the received frame's associated CRC from the communications channel; and

   an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

2. (Original) The system according to claim 1, further comprising:

   a magnetic-disc-storage drive operatively coupled to the first channel node; and

   a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node in a fibre-channel loop in order to transfer data between the first and second channel nodes through the fibre-channel arbitrated-loop communications channel.

3. (Original) The system according to claim 1, further comprising:

   an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

   a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

4. (Original) The system according to claim 3, wherein the integrity apparatus checks and strips away the cyclic-redundancy code while moving the received frame to the off-chip memory, the system further comprising:

a parity-generation circuit that generates and appends parity to the data as the data are moved from the off-chip memory to the on-chip memory.

5. (Original) The system according to claim 3, wherein a data frame devoid of a cyclic-redundancy code is held in the off-chip memory, the system further comprising:

a CRC generator that generates cyclic-redundancy code based on the data frame from the off-chip memory as the data frame is moved into the data-frame buffer, and that places the CRC into the on-chip frame memory with the data frame; and

a transmitter that transmits the data frame, including the generated cyclic-redundancy code, onto the communications channel.

6. (Original) The system according to claim 3, wherein a received frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

7. (Original) The system according to claim 3, wherein a data frame that is to be transmitted is transferred to the on-chip frame memory from the off-chip memory and is stored in the on-chip frame memory with parity but without CRC information.

8. (Original) The system according to claim 7, wherein a received data frame transferred to the on-chip frame memory from the communications channel is stored in the on-chip frame memory with CRC but without parity information.

9. (Original) A disc drive comprising:

a rotatable disc;

a transducer in transducing relationship to the rotating disc;

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel, the channel node operatively coupled to the transducer to communicate data;

an on-chip frame memory located on-chip in the channel node that receives a frame and the received frame's associated CRC from the communications channel; and

an integrity apparatus that uses the received associated CRC for data-integrity checking of the received frame that is in the on-chip frame memory.

10. (Original) The disc drive according to claim 9, further comprising:

an off-chip memory operatively coupled to the on-chip frame memory and the integrity apparatus; and

a verification circuit within the integrity apparatus that verifies the cyclic-redundancy code while moving the received frame from the on-chip memory to the off-chip memory.

11. (Original) A communications method comprising steps of:

(a) supporting a fibre-channel arbitrated-loop communications channel on each of a first port and a second port of a first channel node;

(b) receiving a frame from the communications channel, the received frame including a cyclic-redundancy code that is based on other data in the received frame;

(c) storing the received frame, including the cyclic-redundancy code, into a frame buffer;

(d) moving the received frame to a memory that is separate from the frame buffer; and

(e) checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the separate memory.

12. (Original) The method according to claim 11, wherein the receiving step (b) further includes a step of:

(b)(i) checking the received frame for accuracy by verifying the cyclic-redundancy code while receiving the received frame from the communications channel.

13. (Original) The method according to claim 11, further comprising a step of:

(i) transferring data through the fibre-channel arbitrated-loop communications channel between a magnetic-disc-storage drive that is operatively coupled to the first channel node and a computer system having a second channel node, wherein the second channel node is operatively coupled to the first channel node by the communications channel.

14. (Original) The method according to claim 11, further comprising steps of:

(f) placing a frame that is to be transmitted into an on-chip frame buffer;

(g) generating the cyclic-redundancy code based on data in the frame to be transmitted; and

(h) transmitting the frame to be transmitted, including the cyclic-redundancy code, onto the communications channel.

15. (Original) The method according to claim 14, wherein the placing step (f) further includes steps of:

(f)(i) generating parity for data of the frame to be transmitted;

(f)(ii) adding parity to the data of the frame to be transmitted; and

wherein the moving step (d) further includes a step of

(d)(i) stripping away the cyclic-redundancy code while moving the received frame to the separate memory.

16. (Original) A communications channel system comprising:

a channel node having a first port and a second port, each port supporting a fibre-channel arbitrated-loop communications channel, each communications channel including a cyclic-redundancy code within data transmissions on the communications channel;

a buffer that receives, from the channel node, a frame that includes a cyclic-redundancy code;

an off-chip memory separate from the buffer;

means for moving the received frame from the buffer to the off-chip memory and checking the received frame for accuracy by verifying the cyclic-redundancy code (CRC) while moving the received frame to the off-chip memory.

17. (Original) The system according to claim 16, wherein the means for moving further includes means for stripping away the CRC as the frame is checked and moved to the off-chip memory.

18. (Added) A system comprising:

a first serial device having n ports supporting a serial communications path;

a first memory coupled to the first serial device that is configured to receive a first packet and a first data protection code associated with the first packet from the serial communications path;

an integrity apparatus configured to check a data-integrity of the first packet based on the first data protection code, remove the data protection code from the first packet, and store the first packet to a second memory without storing the first data protection code in the second memory; and

a data protection code generation circuit coupled to the first memory that generates and appends a second data protection code to the first packet when the first packet is moved from the second memory to the first memory.

19. (Added) The system according to claim 18 wherein n comprises one or more.

20. (Added) The system according to claim 18, further comprising:

the first serial device comprising a single chip including the first memory;

a data storage device operatively coupled to the first serial device, the data storage device including the second memory; and

a computer system having a second serial device, wherein the second serial device is operatively coupled to the first serial device in a serial communications path in order to transfer data between the first and second serial devices through the serial communications path.

21. (Added) The system according to claim 18, further comprising:

the second memory operatively coupled to the first memory and the integrity apparatus;

a verification circuit within the integrity apparatus that verifies the data protection code; and

a circuit for moving the first packet from the first memory to the second memory.

22. (Canceled)

23. (Added) The system according to claim 21, further comprising a transmitter configured to transmit the second packet, including the second data protection code, over the serial communications path.

24. (Added) A data storage device, comprising:

a data storage medium;

a single integrated circuit chip operatively coupled to the data storage medium to communicate data, the single integrated circuit chip comprising:

at least one port supporting a serial communications path;

a memory coupled to the at least one port that is adapted to receive a packet and an associated data protection code from external to the data storage device over the serial communications path;

first logic coupled to the memory and configured to check a data-integrity of the packet based on the data protection code, remove the data protection code from the packet, and store the packet without the data protection code to the data storage medium; and

second logic coupled to the memory to generate and append a second data protection code to the packet when the packet is moved from the data storage medium to the memory.

25. (Added) The data storage device according to claim 24, wherein the single integrated circuit chip further comprises:

more than one port supporting a serial communications path;

a number of transceivers equal to the number of ports, each transceiver coupled to one of the ports and configured to receive packets from a data path external to the data storage device and provide the packets as serialized data to a respective port.

26. (Added) A method comprising:

receiving a packet at an interface coupled to a serial communications path, the packet including a data protection code;

storing the packet, including the data protection code, into a buffer;

removing the data protection code from the packet; and

storing the packet without the data protection code to a memory location other than the buffer.

27. (Added) The method according to claim 26, wherein receiving further comprises checking the packet for accuracy by verifying the data protection code after receiving the packet from the serial communications path.

28. (Added) The method according to claim 26, further comprises checking the packet for accuracy by verifying the data protection code while storing the packet to the memory location.

29. (Added) The method according to claim 26, further comprising:

retrieving the packet from the memory location and storing it in the buffer;

generating a second data protection code based on data in the packet; and

transmitting the packet, including the second data protection code, onto the serial communications path.

30. (Added) The method according to claim 29, further comprising:

generating parity for data in the packet to be transmitted; and

adding the parity to the data in the packet to be transmitted.

31. (Added) A system comprising:

at least one port, each port supporting a serial communications path;

a buffer coupled to the at least one port that receives, from the serial communications path, a packet that includes a first data protection code;

a memory separate from the buffer;

means for checking the packet for accuracy by verifying the first data protection code and storing the packet without the first data protection code to the memory;

means for retrieving the packet without the first data protection code from the memory;

means for generating and appending a second data protection code to the packet when the packet is retrieved from the memory; and

means for sending the packet with the second data protection code over the serial communications path.

32. (Added) The system according to claim 31, wherein the means for checking and storing further comprises logic operable to check the received packet for accuracy by verifying the data protection code and store the packet without the data protection code to the memory.